FIG. 1

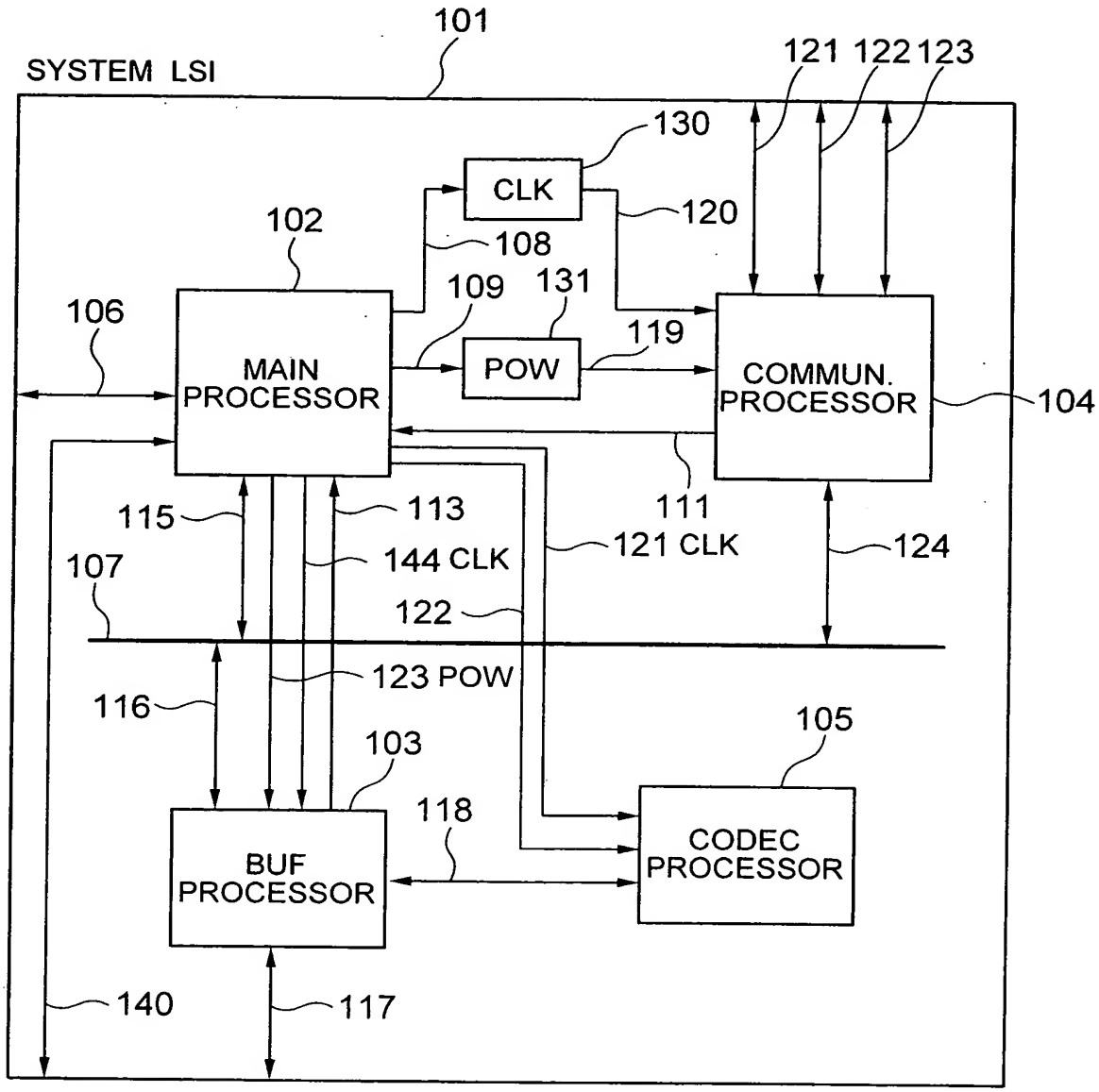
101
SYSTEM LSI
121 122 123
130
CLK
120
102
108
109
131
106
MAIN PROCESSOR
POW
119
COMMUN. PROCESSOR
104
111
115
113
121 CLK
124
107
144 CLK
122
123 POW
116
105
103
118
BUF PROCESSOR
CODEC PROCESSOR
140
117

FIG. 2

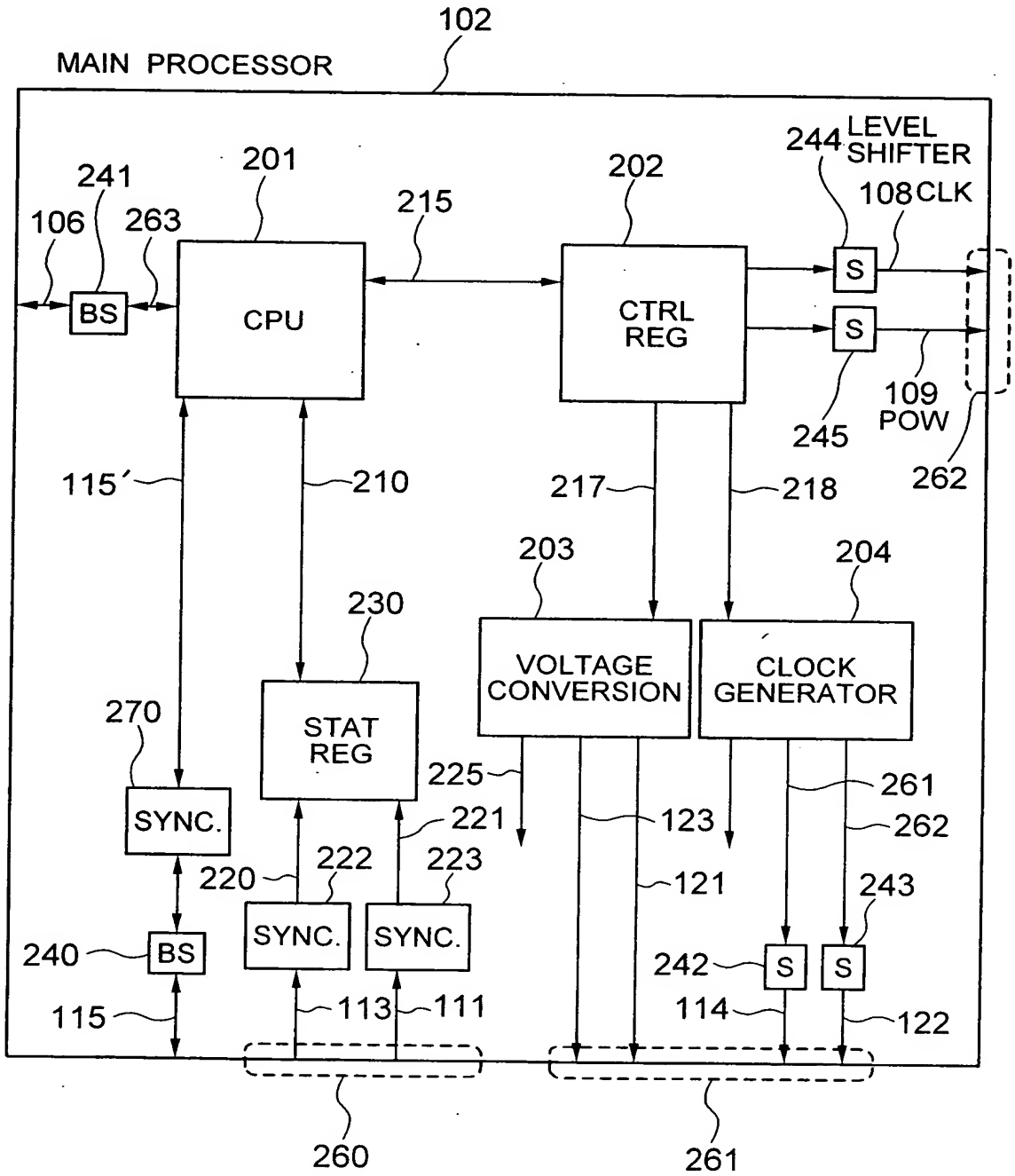
102
MAIN PROCESSOR
241
201
202
244
LEVEL SHIFTER
106
263
215
108
CLK
BS
CPU
CTRL REG
S
S
109
POW
245
262
115'
210
217
218
203
204
230
VOLTAGE CONVERSION
CLOCK GENERATOR
270
STAT REG
225
261
SYNC.
221
123
262
220
222
223
121
243
240
BS
SYNC.
SYNC.
242
S
S
115
113
111
114
122
260
261

FIG. 3

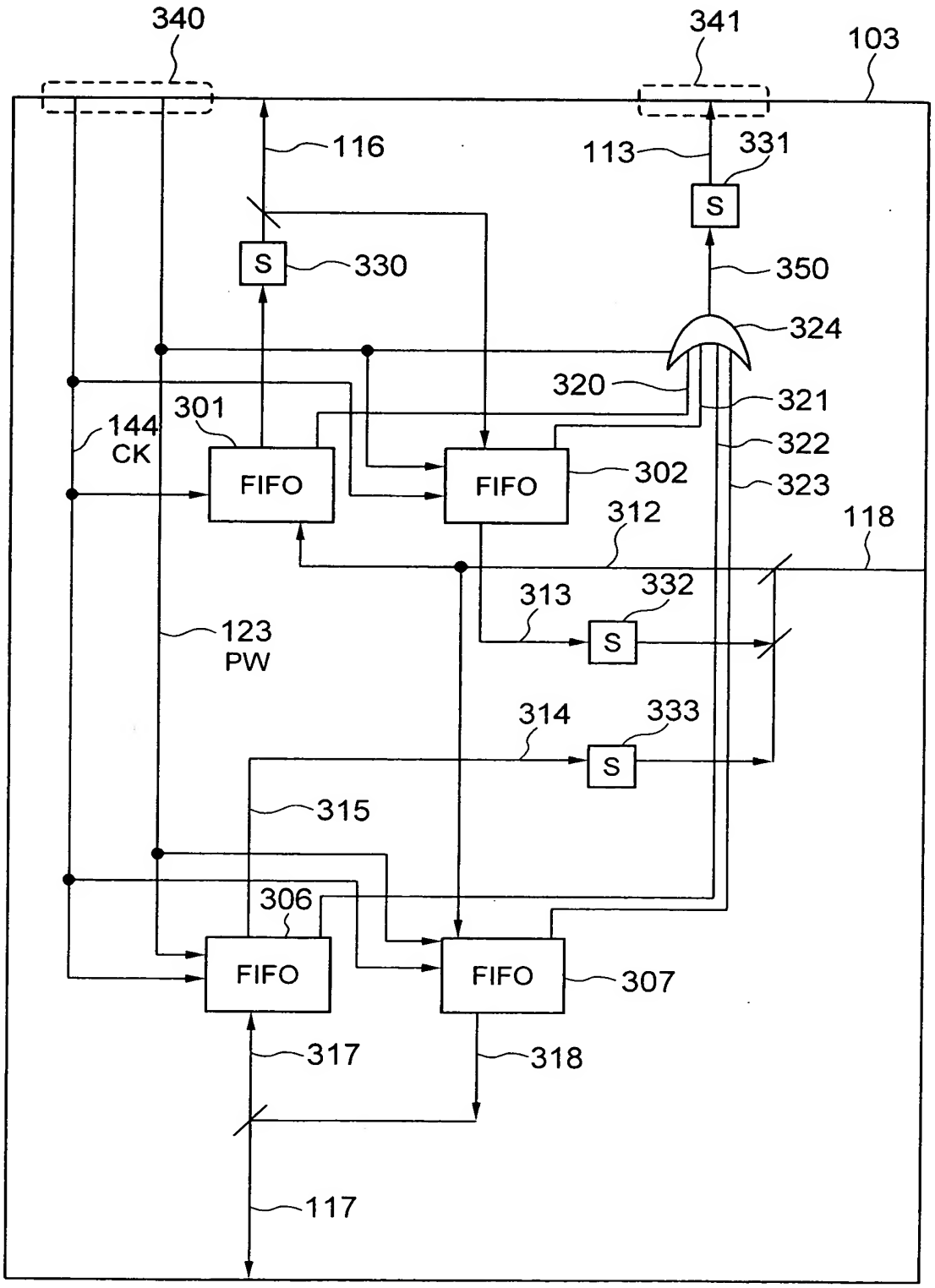
340
341
103
116
113
331
S
330
350
324
320
321
322
323
301
144
CK
FIFO
FIFO
302
312
118
313
332
123
PW
314
333
315
306
FIFO
FIFO
307
317
318
117

FIG. 4A

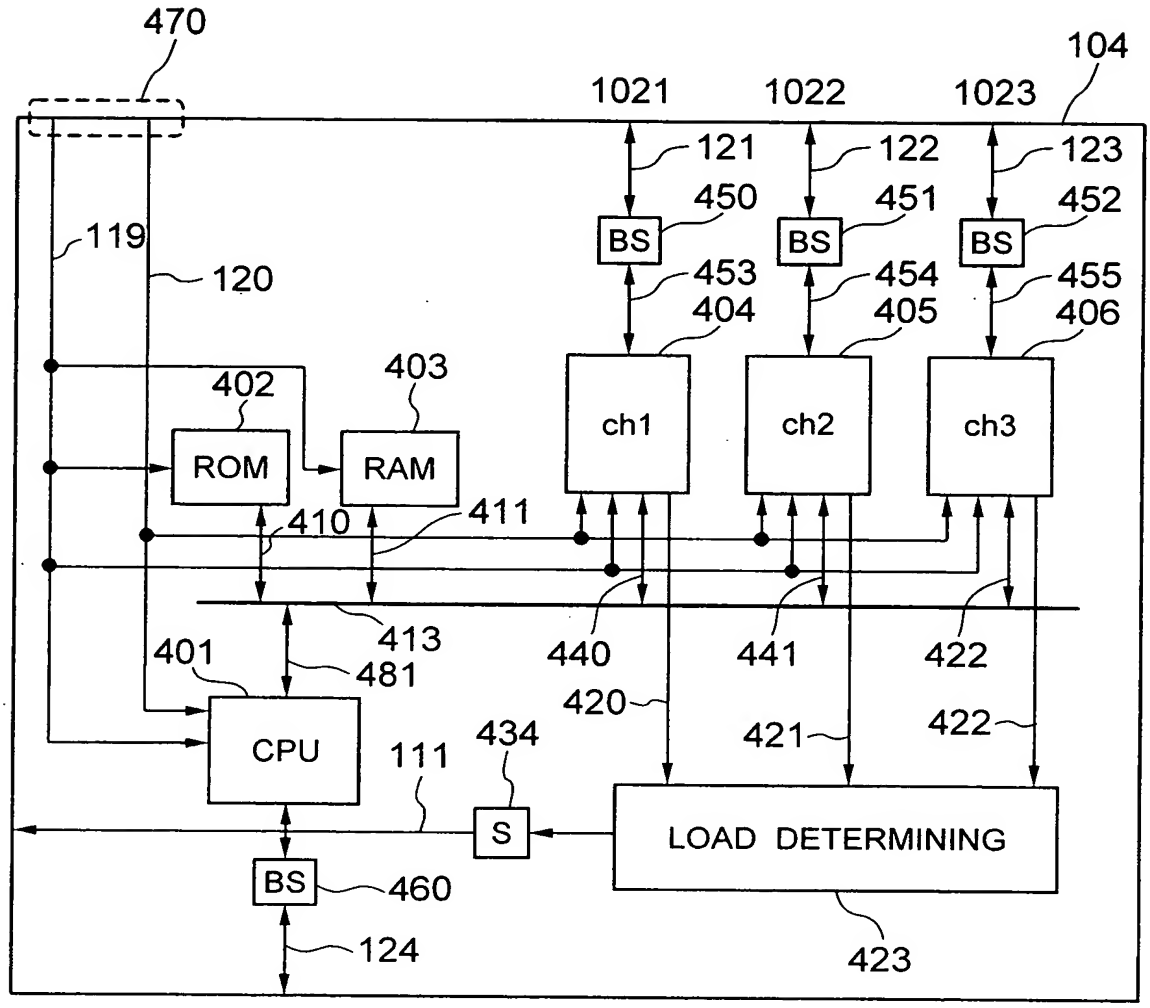
470
104
1021
1022
1023
121
122
123
450
451
452
BS
BS
BS
119
120
453
454
455
404
405
406
403
402
ch1
ch2
ch3
ROM
RAM
410
411
413
440
441
422
401
481
420
421
422
CPU
111
434
S
LOAD DETERMINING
BS
460
124
423

FIG. 4B

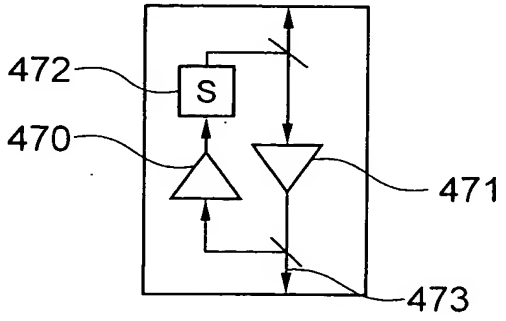
472
S
470
471
473

FIG. 5

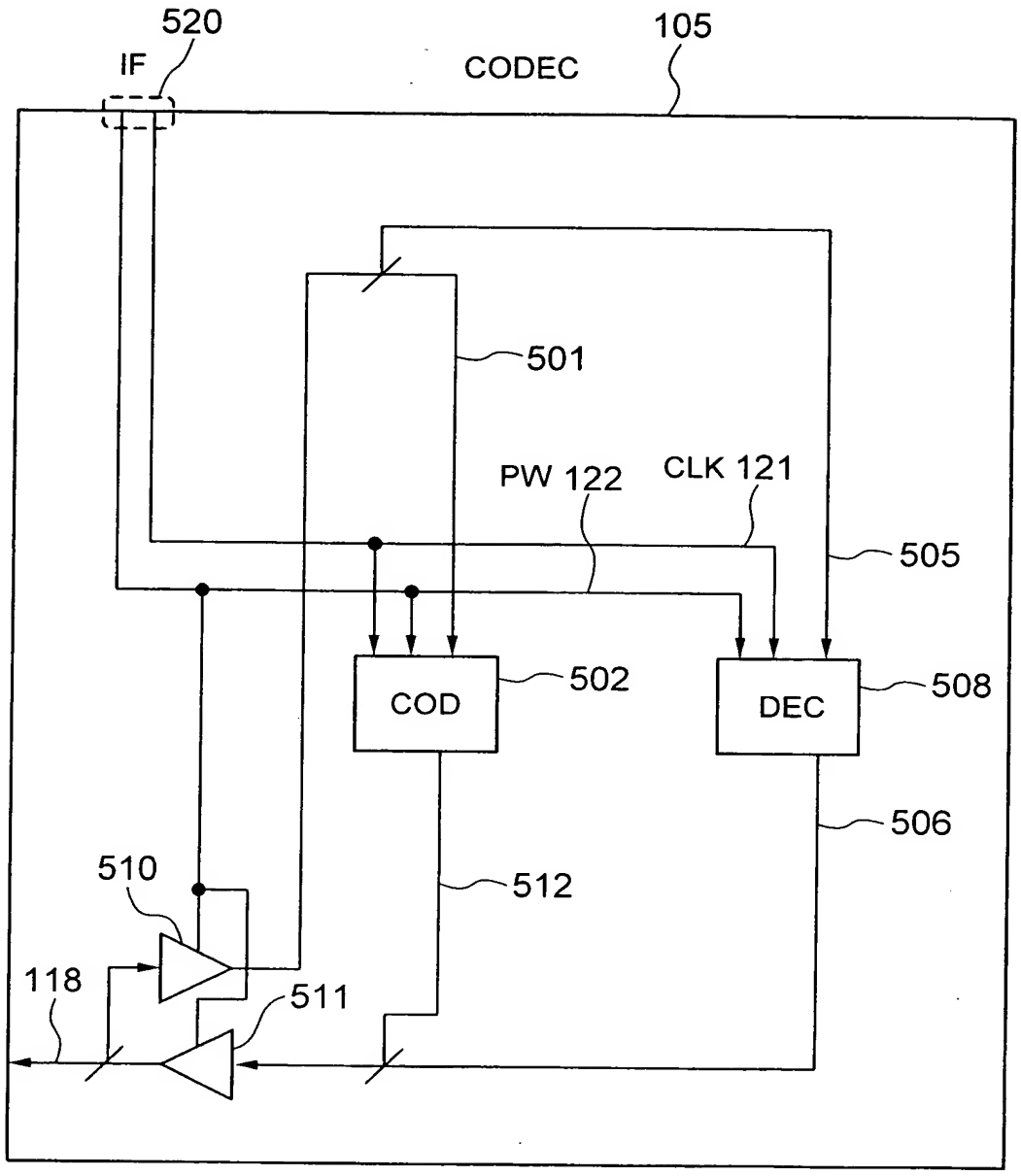
520
IF
CODEC
105
501
PW 122
CLK 121
505
COD
502
DEC
508
506
510
512
118
511

FIG. 6

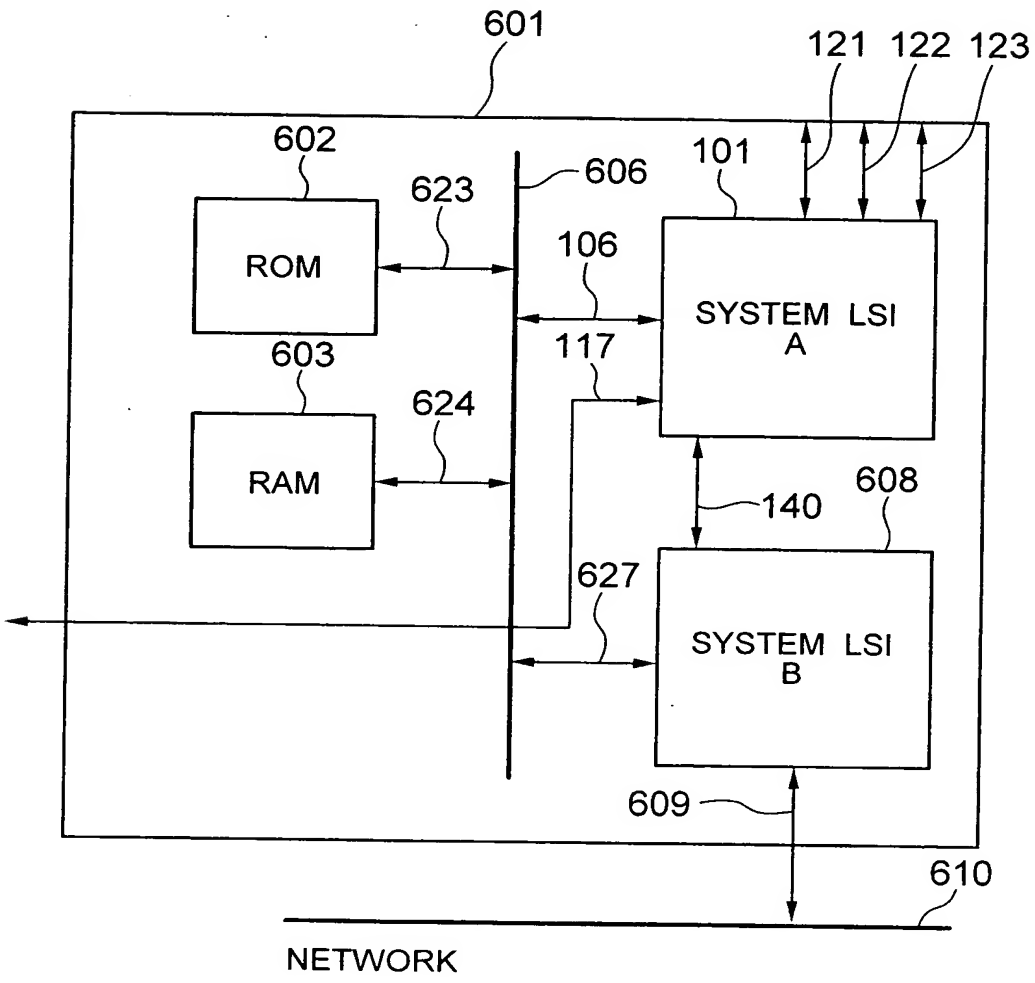
601
121
122
123
602
606
101
623
ROM
106
SYSTEM LSI A
603
117
624
RAM
140
608
627
SYSTEM LSI B
609
610
NETWORK

FIG. 7

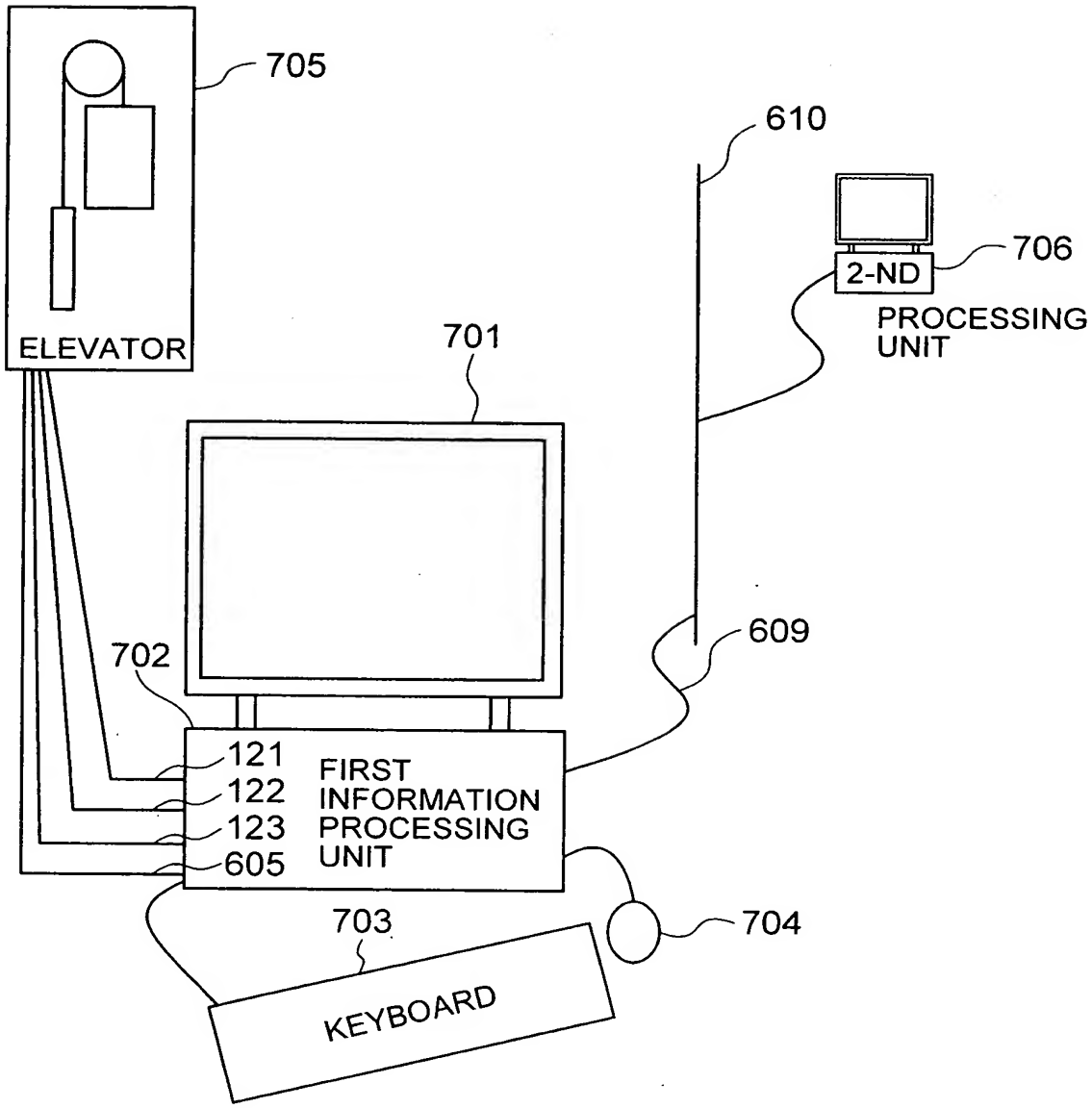
705
610
706
2-ND
PROCESSING UNIT
ELEVATOR
701
609
702
121
122
123
605
FIRST INFORMATION PROCESSING UNIT
703
704
KEYBOARD

FIG. 8

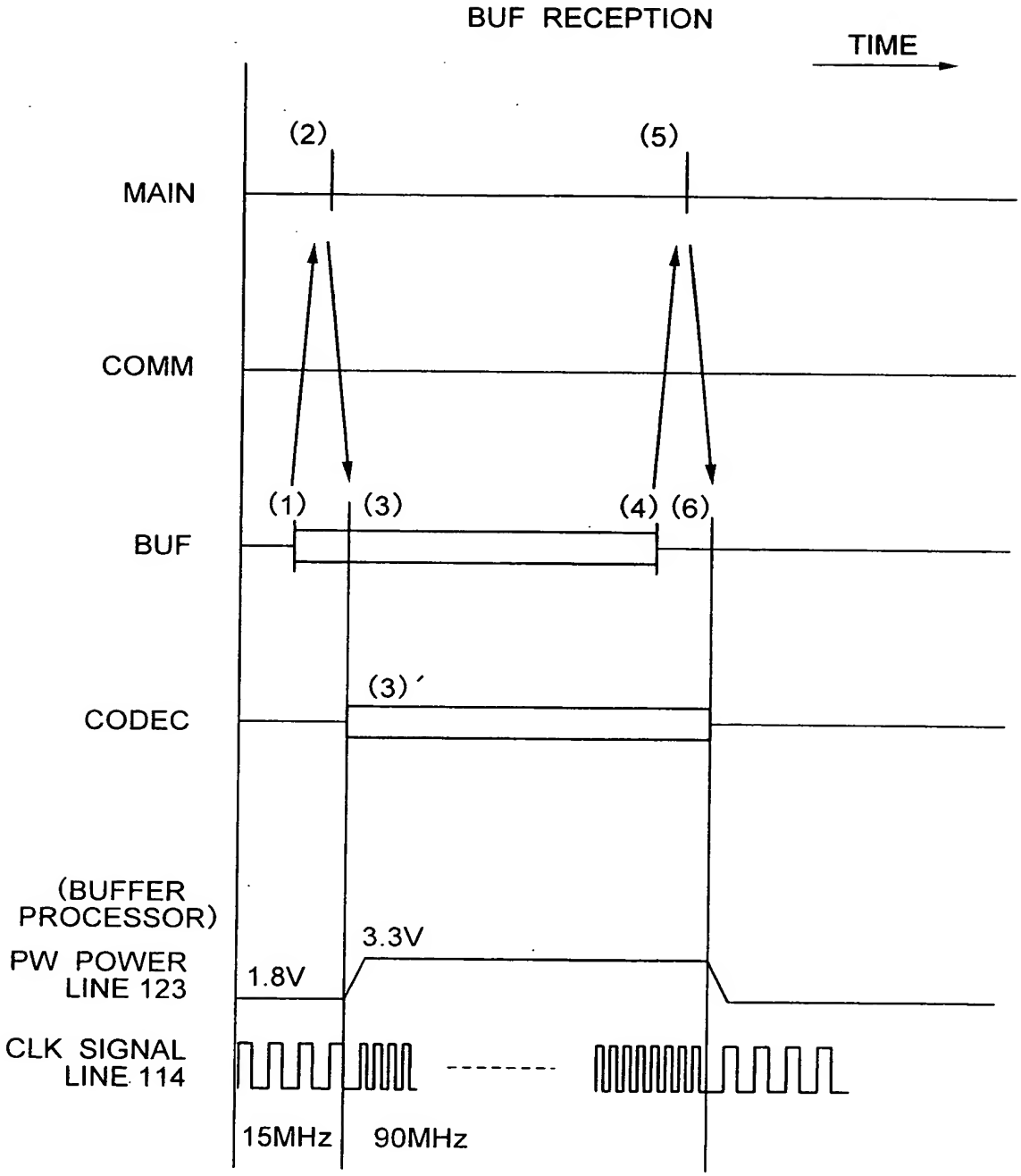
BUF RECEPTION
TIME
(2)
(5)
MAIN
COMM
(1)
(3)
(4)
(6)
BUF
(3)´
CODEC
(BUFFER PROCESSOR)
PW POWER LINE 123
3.3V
1.8V
CLK SIGNAL LINE 114
15MHz
90MHz

FIG. 9

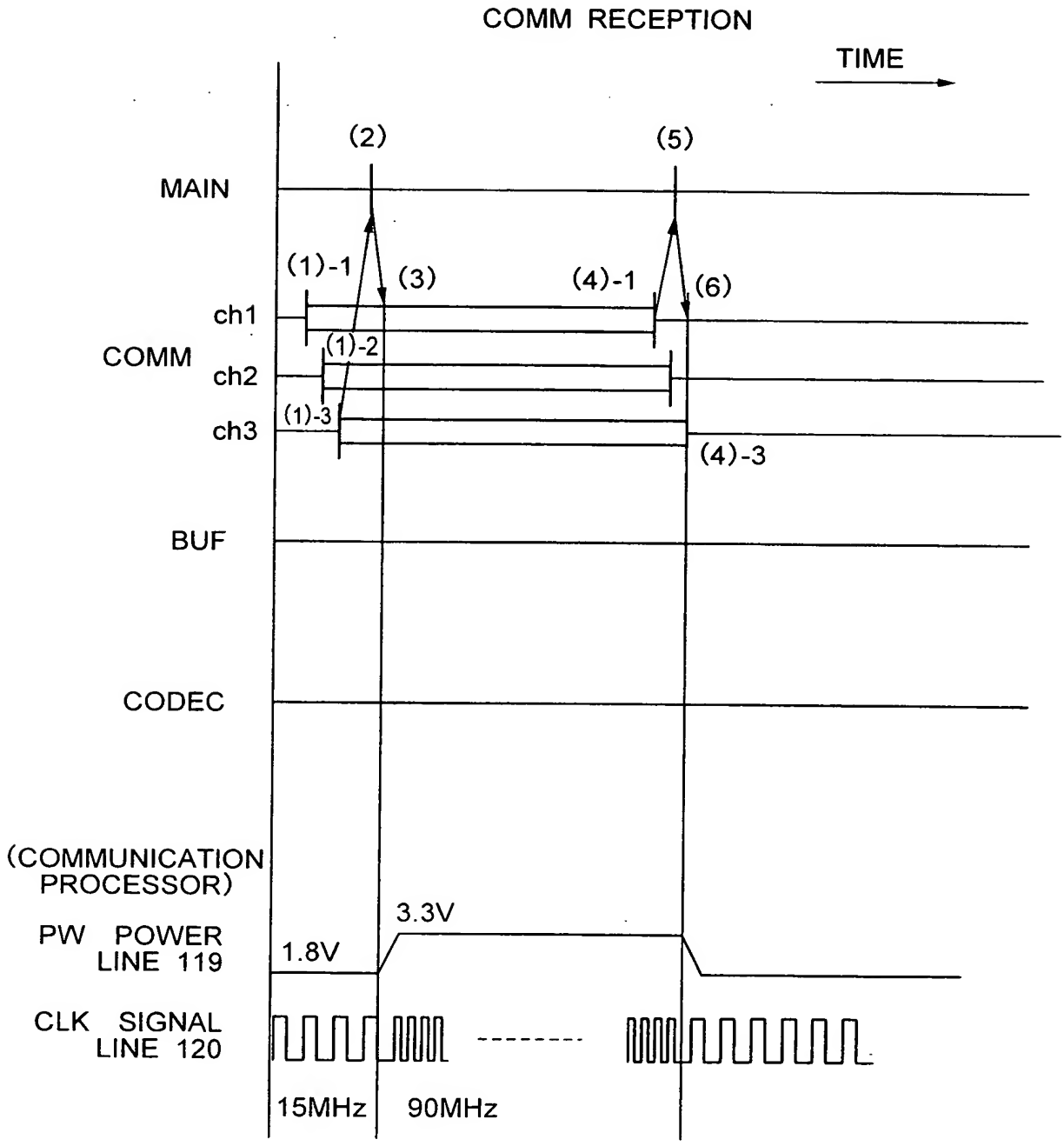
COMM RECEPTION
TIME
(2)
(5)
MAIN
(1)-1
(3)
(4)-1
(6)
ch1
COMM
(1)-2
ch2
(1)-3
ch3
(4)-3
BUF
CODEC
(COMMUNICATION PROCESSOR)
PW POWER LINE 119
3.3V
1.8V
CLK SIGNAL LINE 120
15MHz
90MHz

FIG. 10

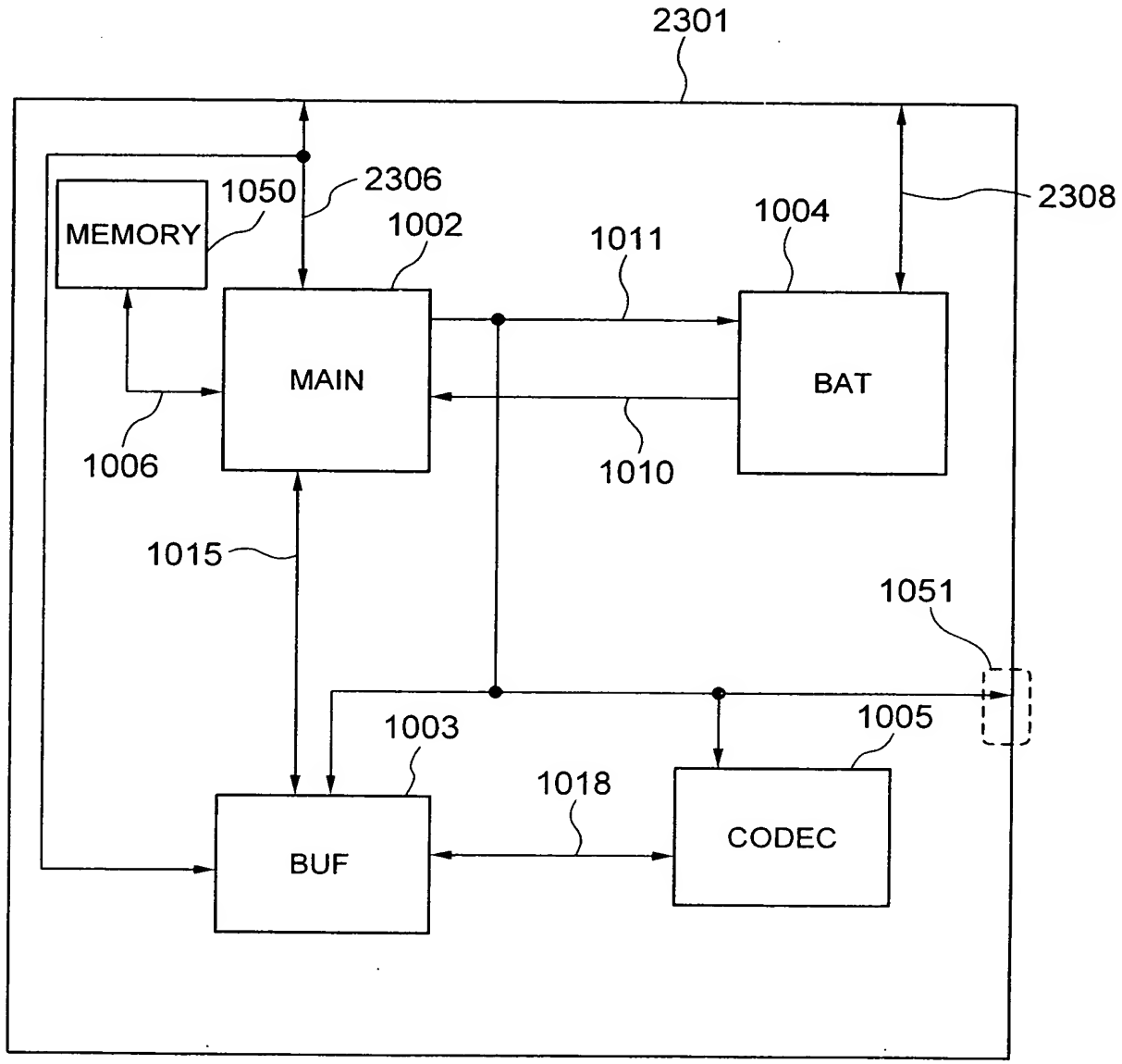
2301
2306
1050
MEMORY
1002
1011
1004
2308
MAIN
BAT
1006
1010
1015
1051
1003
1005
1018
BUF
CODEC

FIG. 11

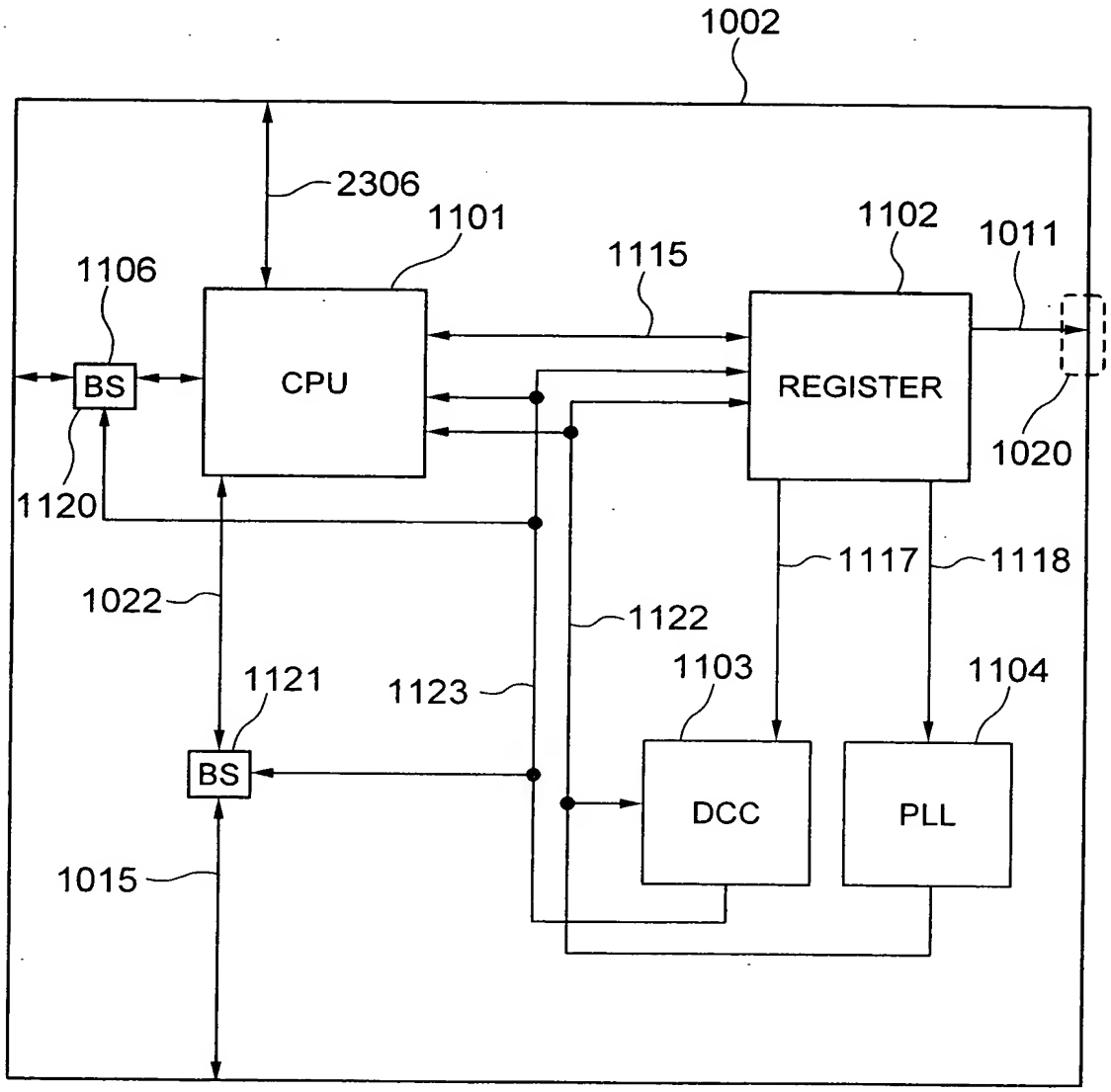
1002
2306
1101
1102
1011
1115
1106
CPU
REGISTER
BS
1020
1120
1117
1118
1022
1122
1121
1123
1103
1104
BS
DCC
PLL
1015

FIG. 12

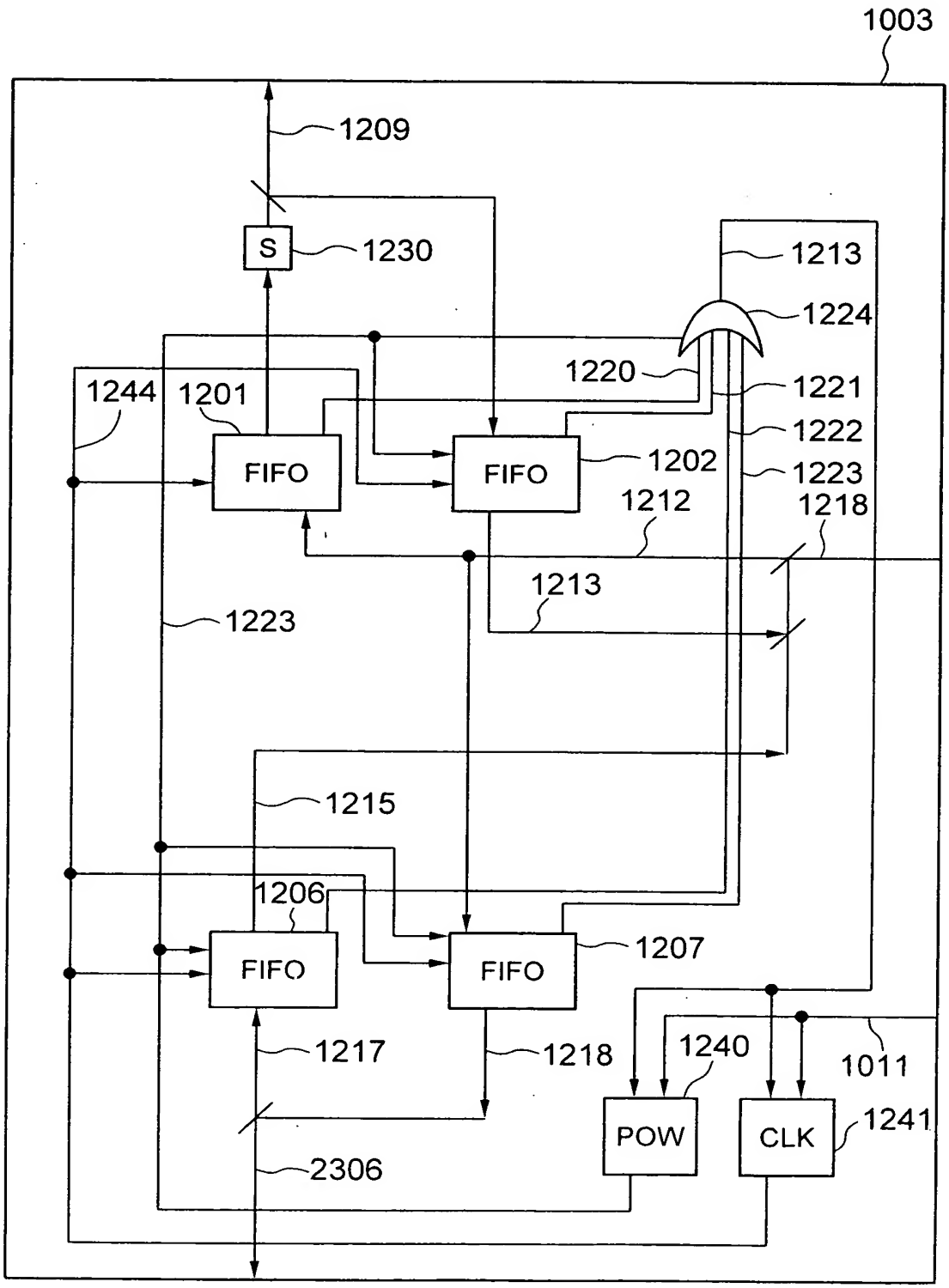
1003
1209
S
1230
1213
1224
1220
1221
1222
1223
1244
1201
FIFO
FIFO
1202
1212
1218
1213
1223
1215
1206
FIFO
FIFO
1207
1217
1218
1240
1011
POW
CLK
1241
2306

FIG. 13

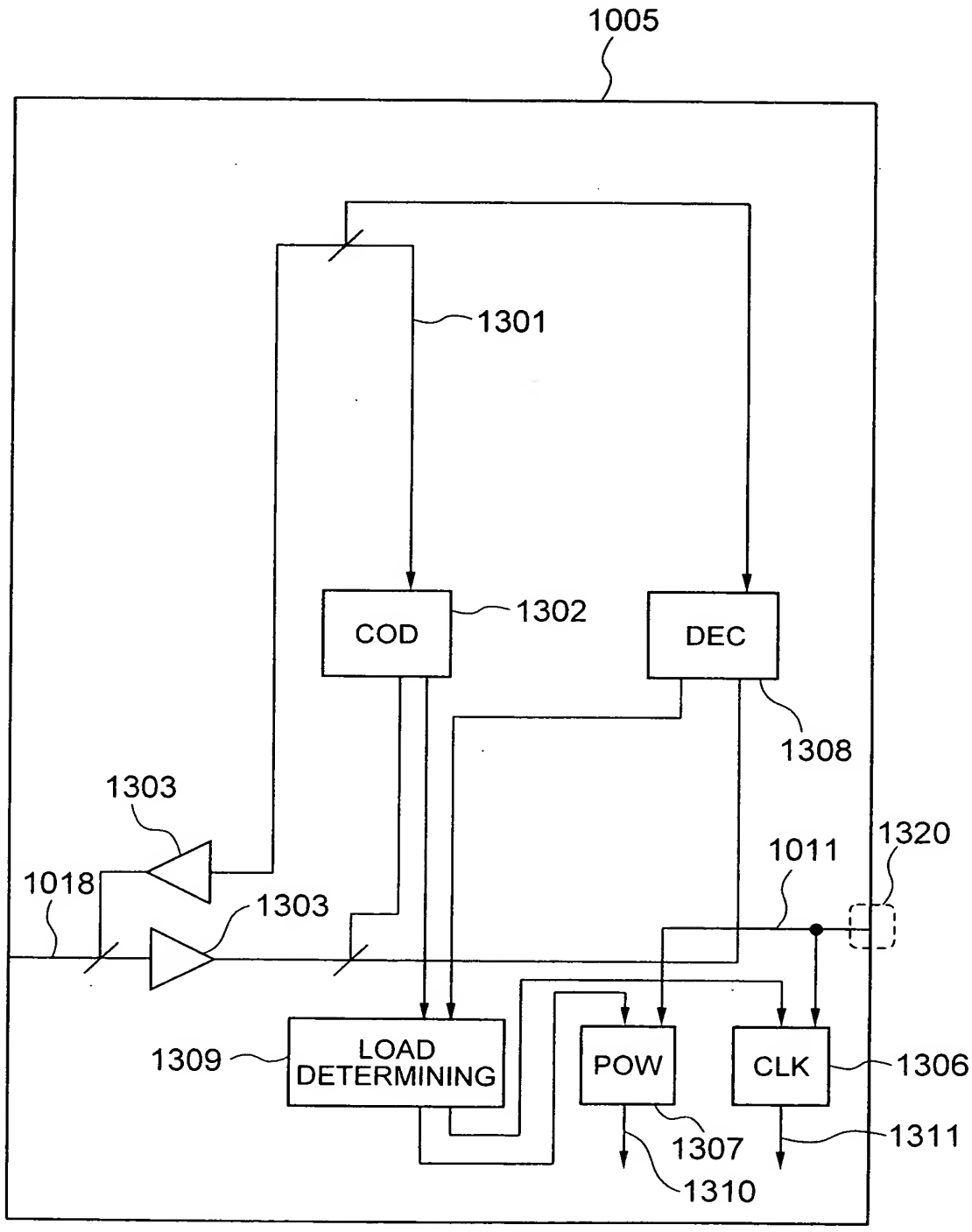
1005
1301
COD
1302
DEC
1308
1303
1018
1303
1011
1320
1309
LOAD DETERMINING
POW
CLK
1306
1307
1311
1310

FIG. 14A

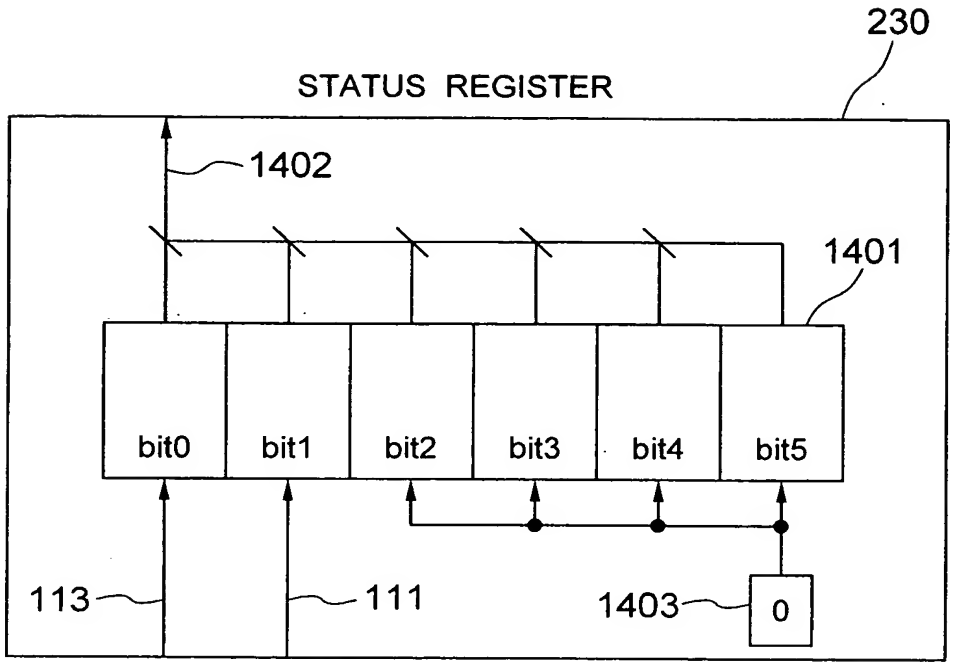

FIG. 14B

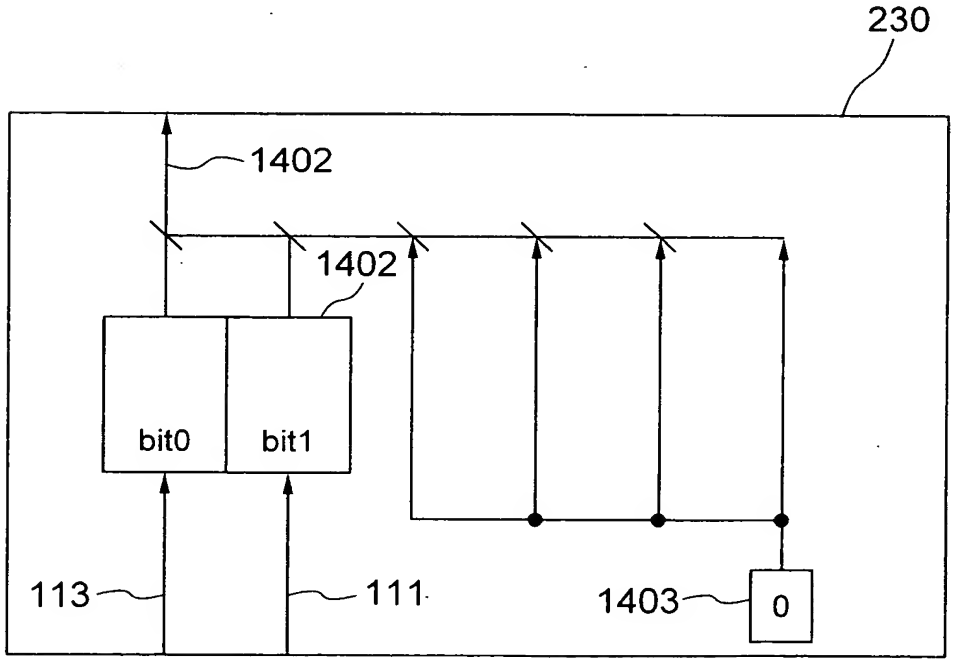

FIG. 15

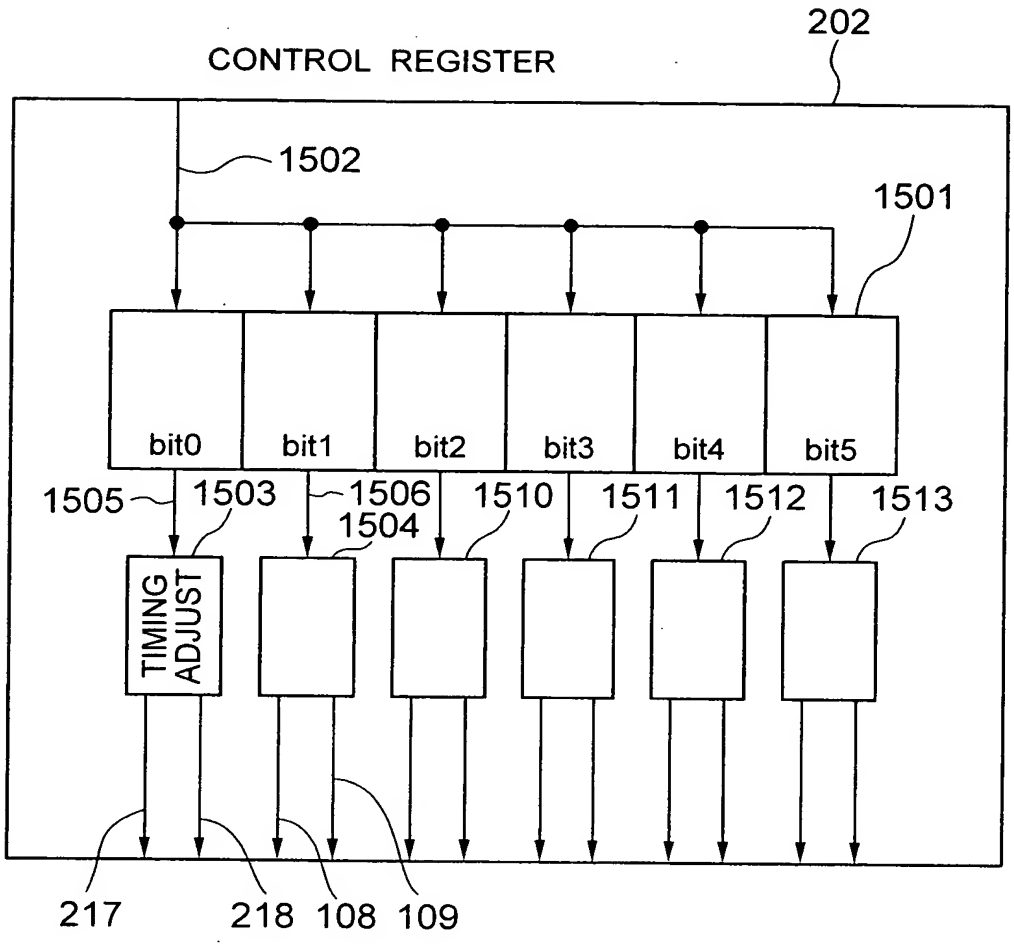
CONTROL REGISTER
202
1502
1501
bit0
bit1
bit2
bit3
bit4
bit5
1505
1503
1506
1504
1510
1511
1512
1513
TIMING ADJUST
217
218
108
109

FIG. 16

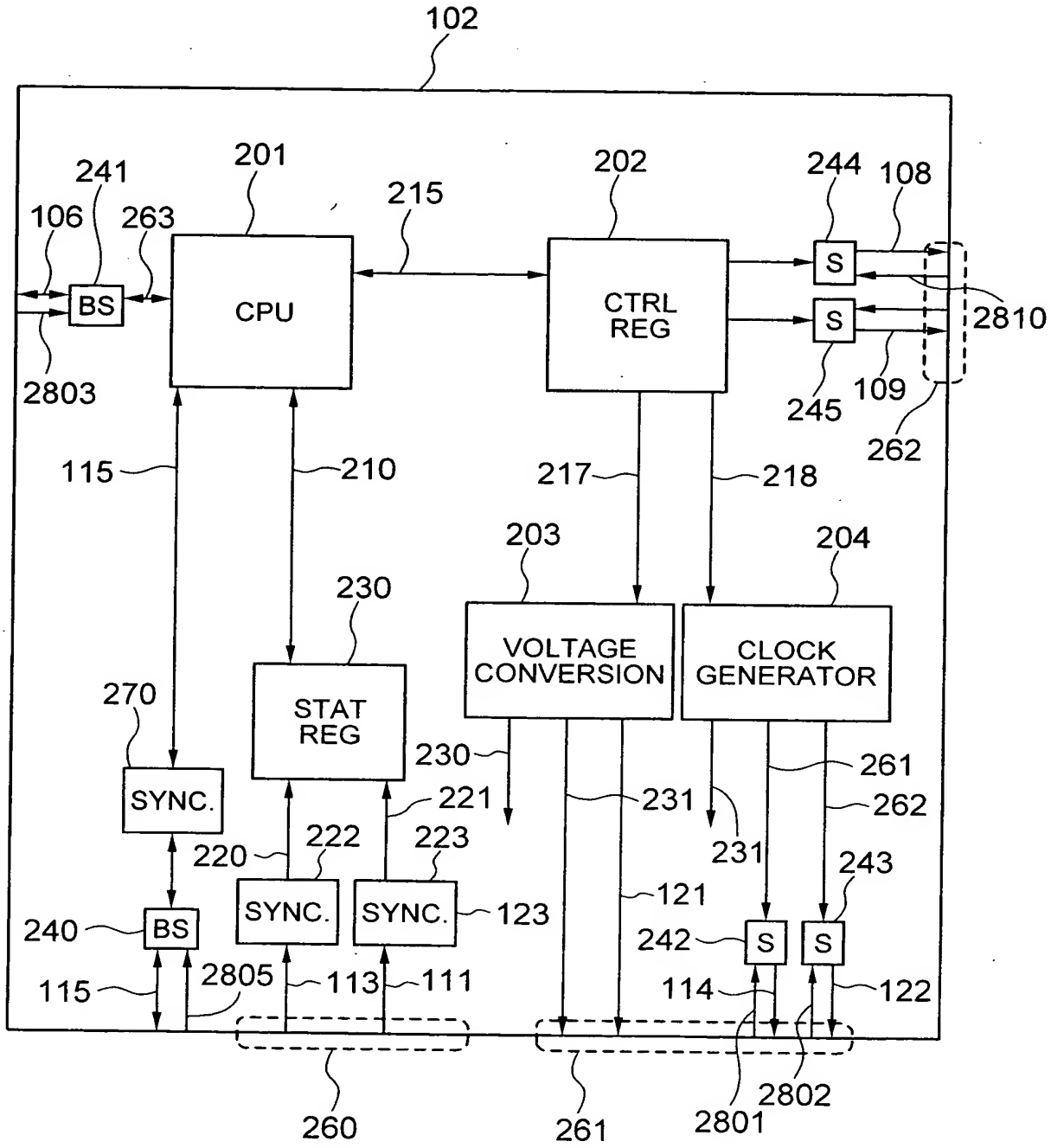
102
241
201
202
244
108
106
263
215
BS
CPU
CTRL REG
S
S
2810
2803
245
109
262
115
210
217
218
203
204
230
VOLTAGE CONVERSION
CLOCK GENERATOR
270
STAT REG
230
261
SYNC.
221
231
231
262
220
222
223
243
SYNC.
SYNC.
123
121
240
BS
242
S
S
115
2805
113
111
114
122
260
261
2801
2802

FIG. 17

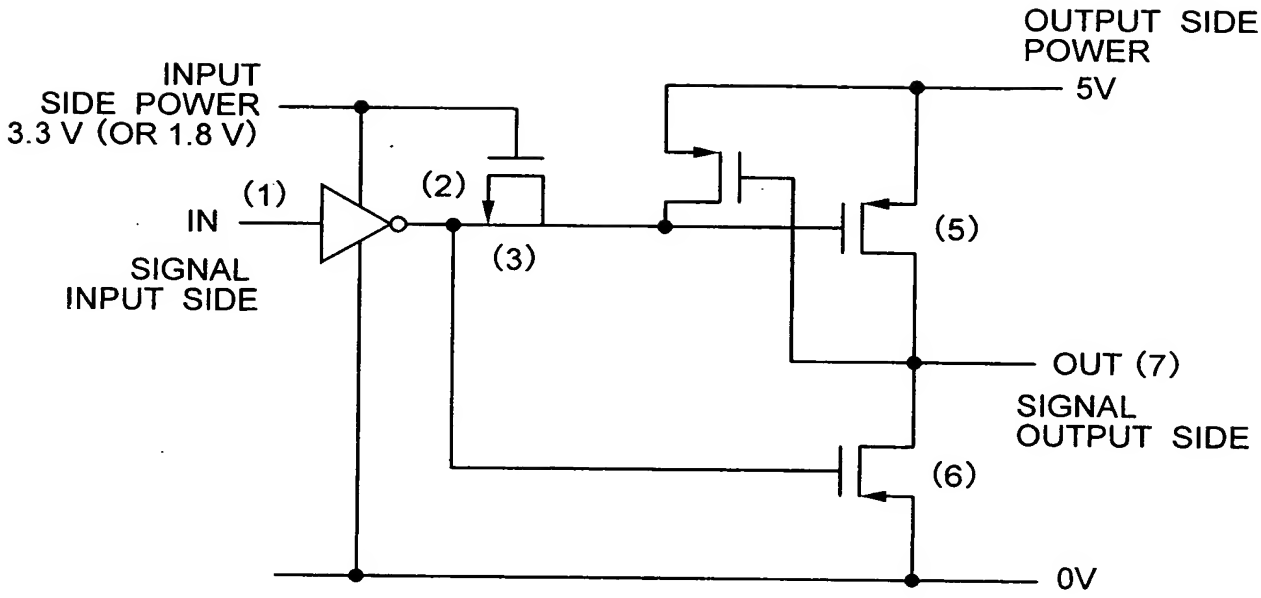
OUTPUT SIDE
POWER
5V
INPUT
SIDE POWER
3.3 V (OR 1.8 V)
(1)
IN
SIGNAL
INPUT SIDE
(2)
(3)
(5)
OUT (7)
SIGNAL
OUTPUT SIDE
(6)
0V

FIG. 18

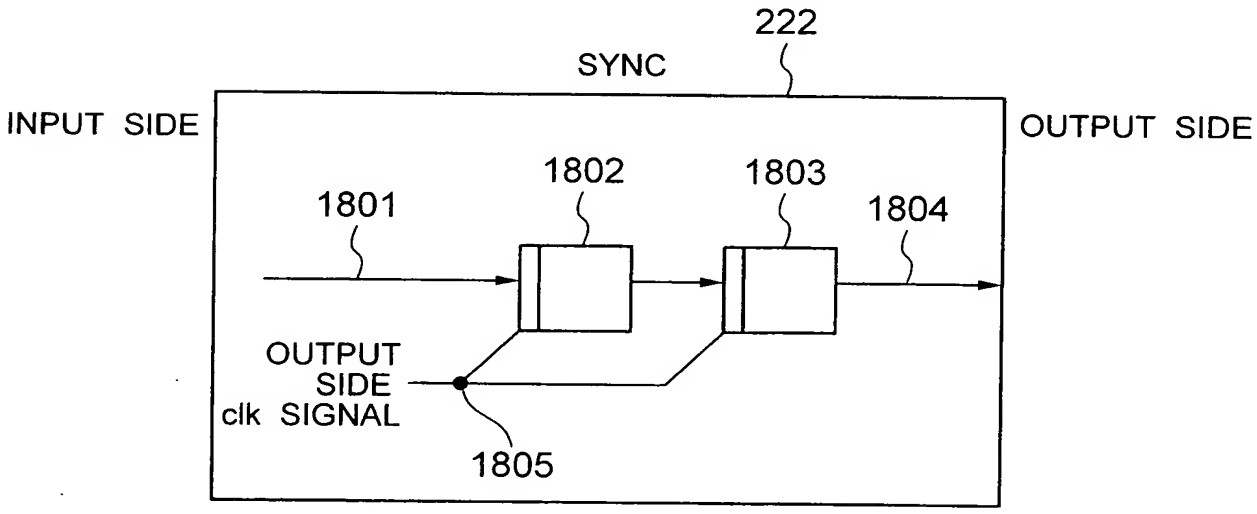
222
SYNC
INPUT SIDE
OUTPUT SIDE
1801
1802
1803
1804
OUTPUT
SIDE
clk SIGNAL
1805

FIG. 19

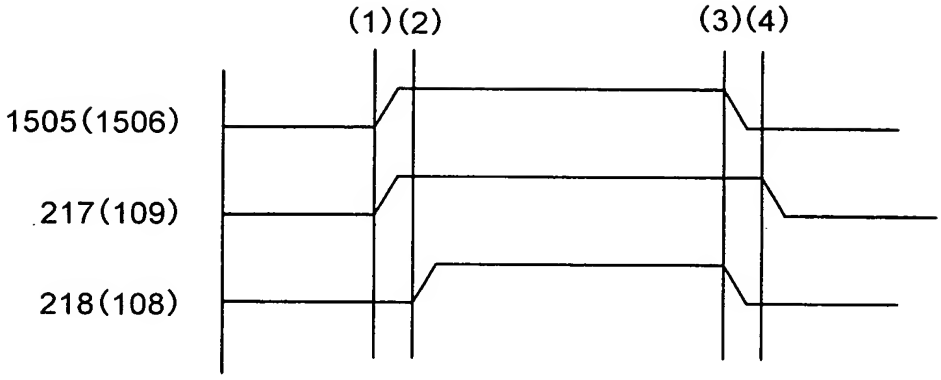

FIG. 20

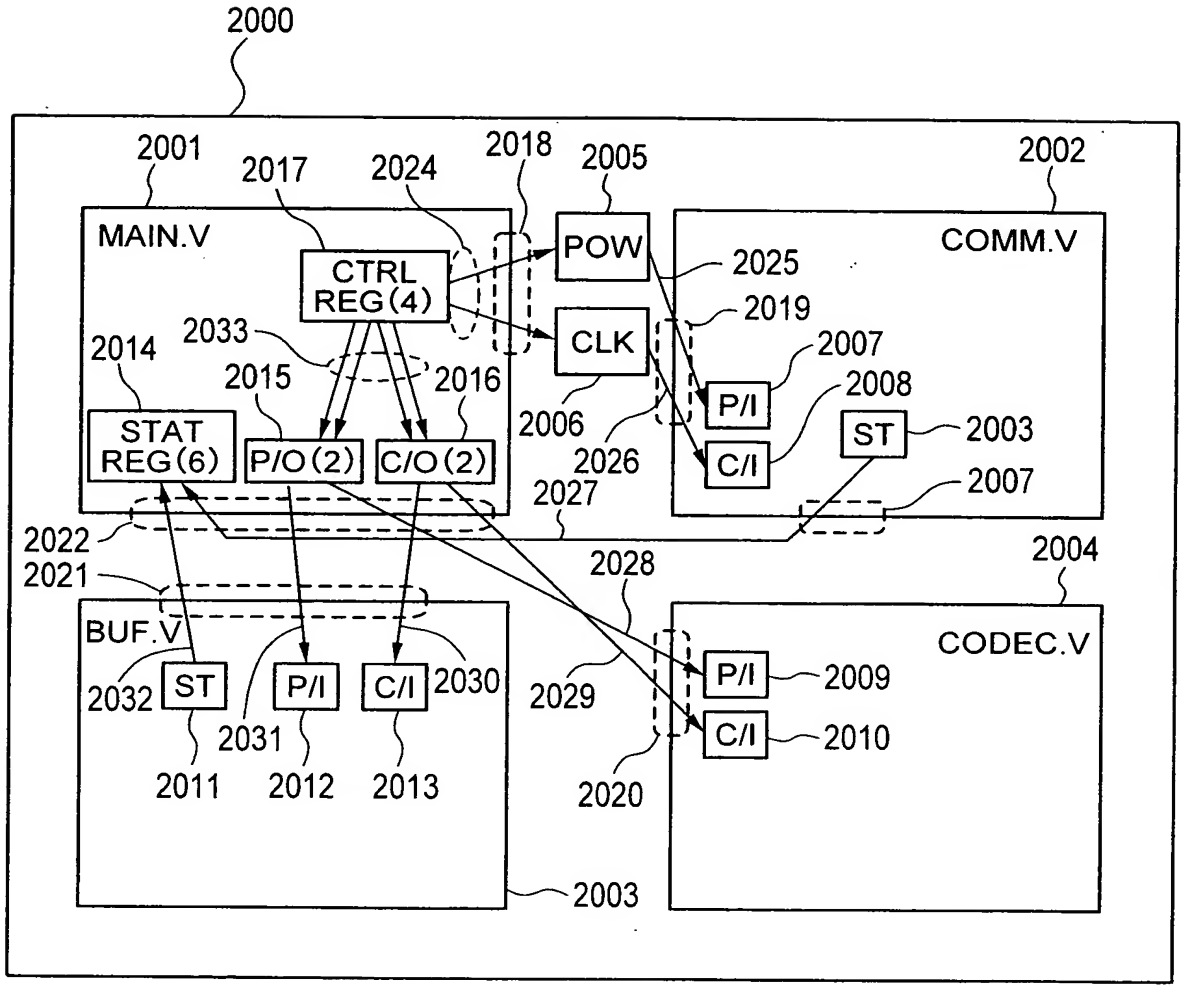
2000
2001
2017
2024
2018
2005
2002
MAIN.V
CTRL REG(4)
POW
COMM.V
2025
2019
2033
CLK
2007
2014
2015
2016
2008
P/I
STAT REG(6)
P/O(2)
C/O(2)
2006
2026
ST
2003
C/I
2007
2027
2022
2028
2004
2021
BUF.V
CODEC.V
2032
ST
P/I
C/I
2030
2029
P/I
2009
2031
C/I
2010
2011
2012
2013
2020
2003

FIG. 21A

```
1: MODULE MAIN(SIG106,···,
2: //FOR POWER CONTROL INTERFACE
3:                SIG113,SIG111,
4:                SIG123,SIG121,
5:                SIG14,SIG122,
6:                SIG108,SIG109,
7: INOUT SIG106,···,
8: INPUT SIG113,SIG111,···,
9: OUTPUT SIG114,SIG122,SIG123,SIG121,···,
          :
          :        } CIRCUIT DESCRIPTION
          :
10: ENDMODULE
```

FIG. 21B

```
1: MODULE BUF(SIG117,SIG118,
2: //FOR POWER CONTROL INTERFACE
3:                SIG144,SIG123,
4:                SIG113,
5: INOUT SIG116,SIG117,SIG118;
6: INPUT SIG123,SIG144;
7: OUTPUT SIG113;
          :
          :        } CIRCUIT DESCRIPTION
          :
8:  ENDMODULE
```

FIG. 22

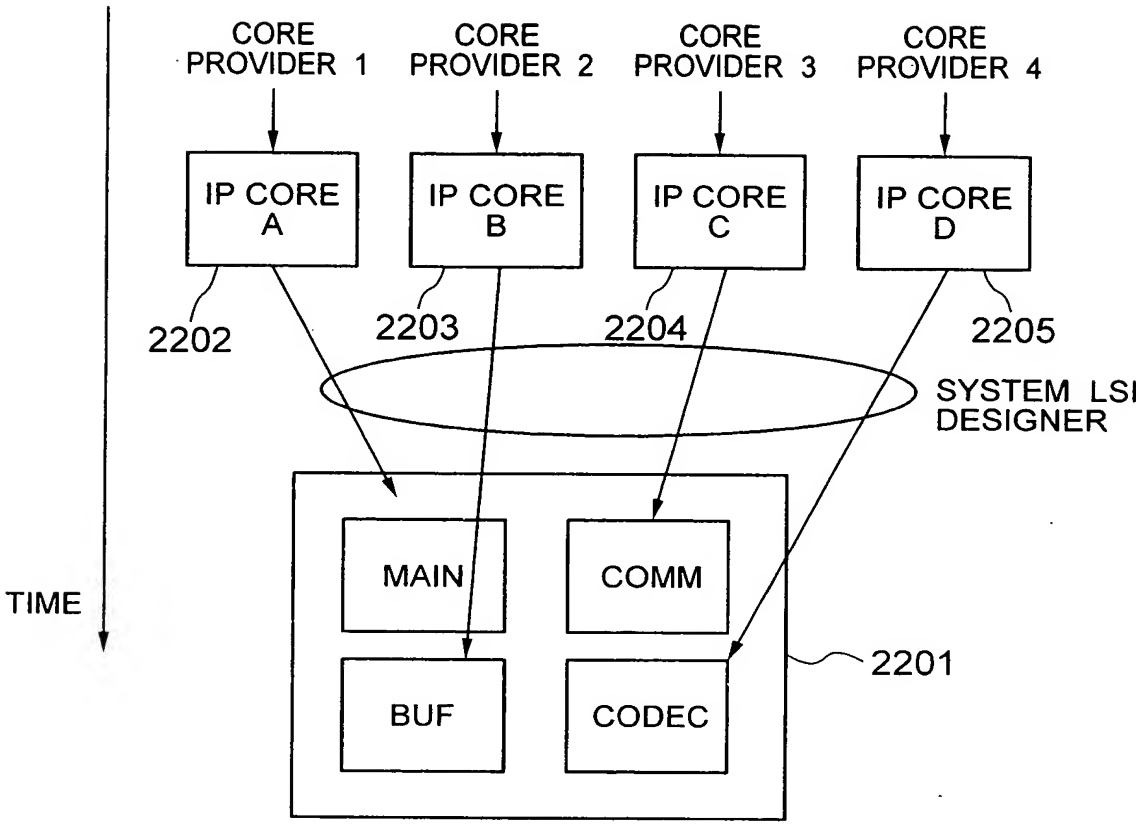
CORE PROVIDER 1
CORE PROVIDER 2
CORE PROVIDER 3
CORE PROVIDER 4
IP CORE A
IP CORE B
IP CORE C
IP CORE D
2202
2203
2204
2205
SYSTEM LSI DESIGNER
TIME
MAIN
COMM
BUF
CODEC
2201

FIG. 23

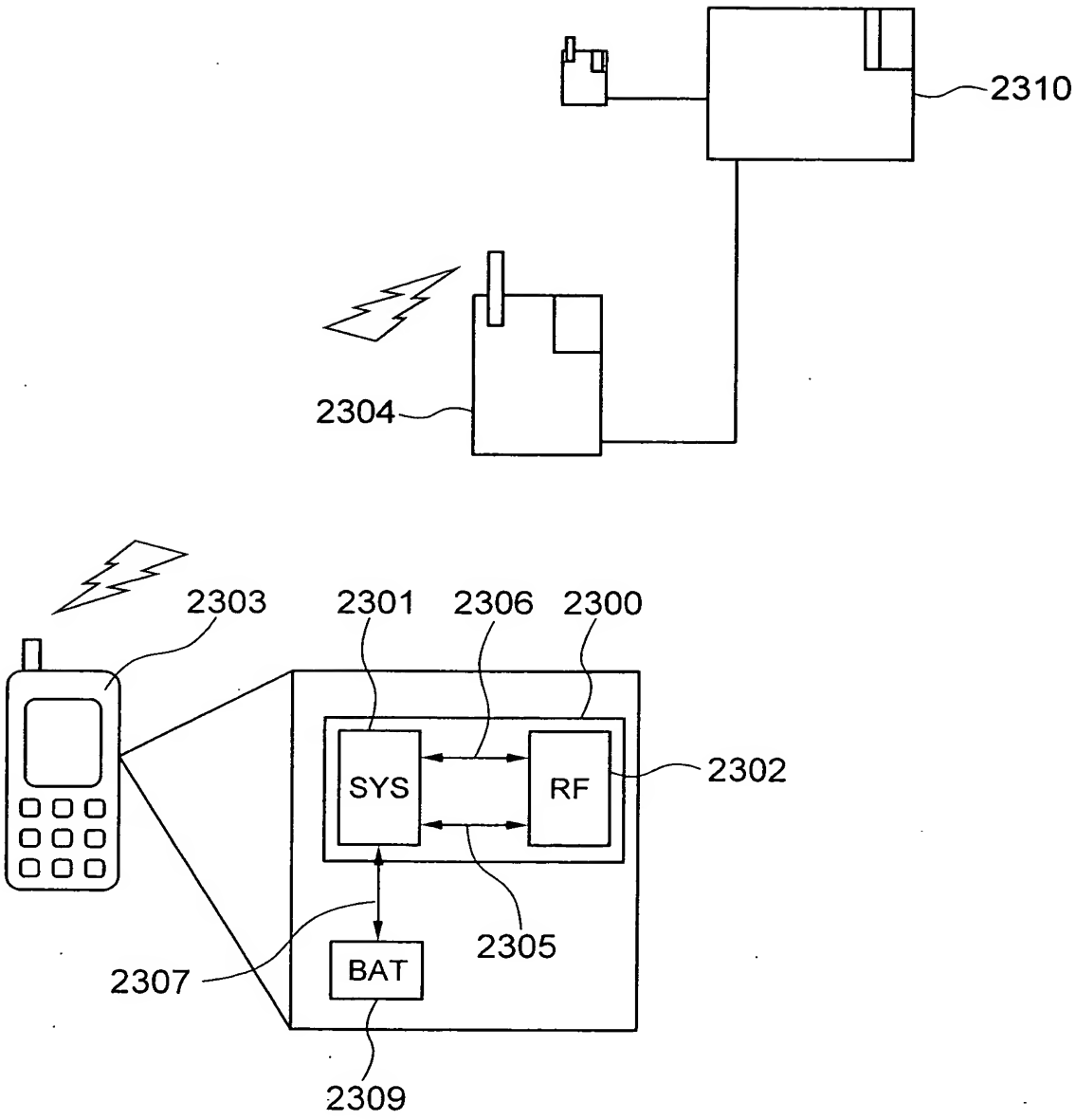

FIG. 24

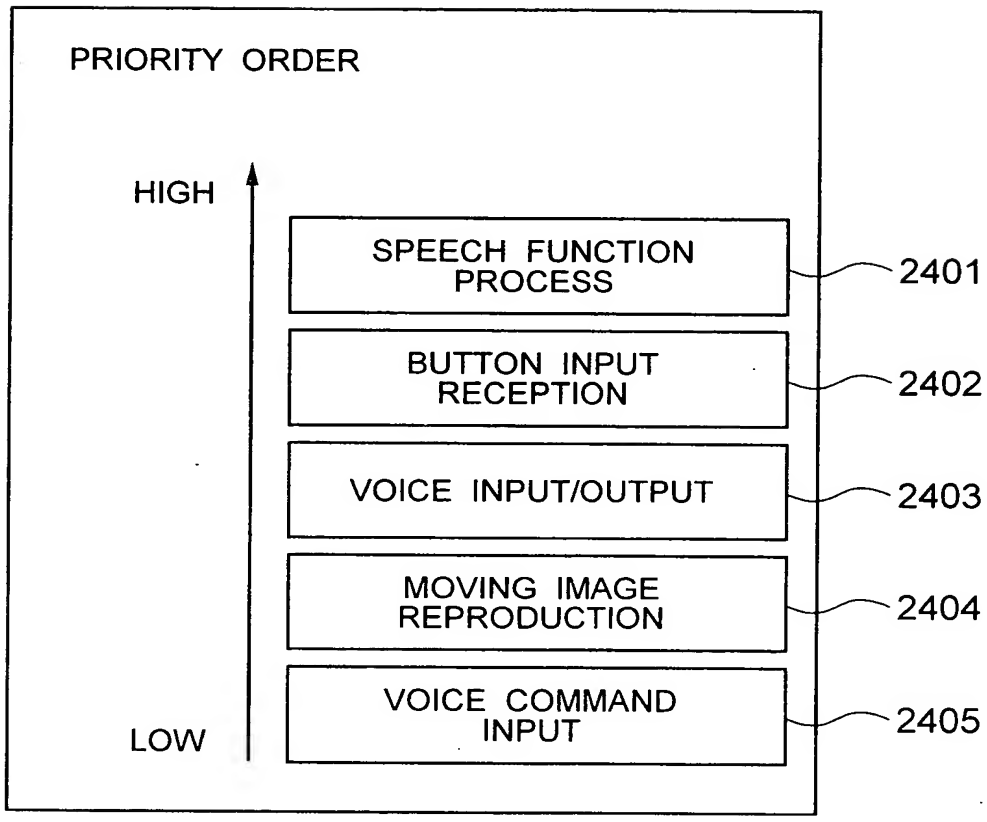
PRIORITY ORDER
HIGH
LOW
SPEECH FUNCTION PROCESS
BUTTON INPUT RECEPTION
VOICE INPUT/OUTPUT
MOVING IMAGE REPRODUCTION
VOICE COMMAND INPUT
2401
2402
2403
2404
2405

FIG. 25

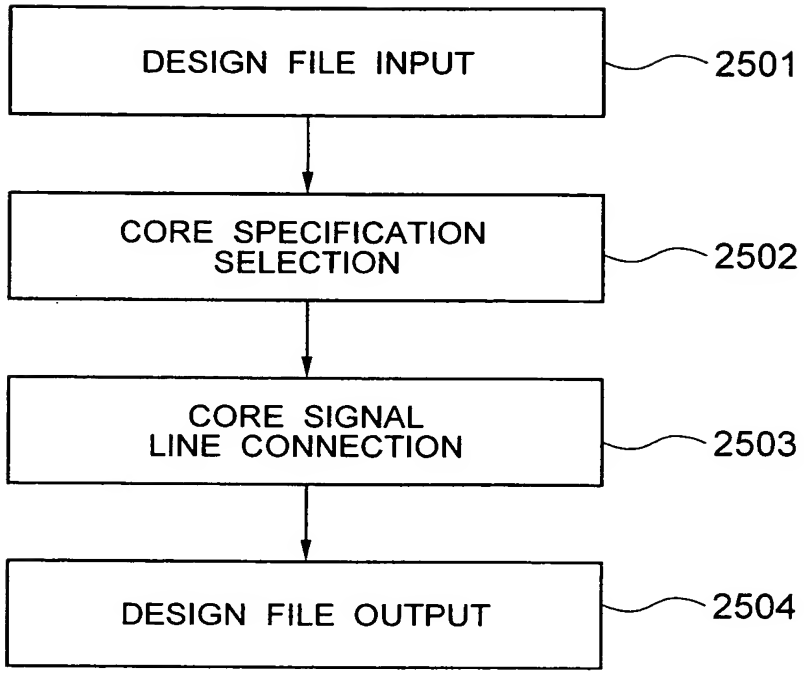
DESIGN FILE INPUT
2501
CORE SPECIFICATION SELECTION
2502
CORE SIGNAL LINE CONNECTION
2503
DESIGN FILE OUTPUT
2504

FIG. 26

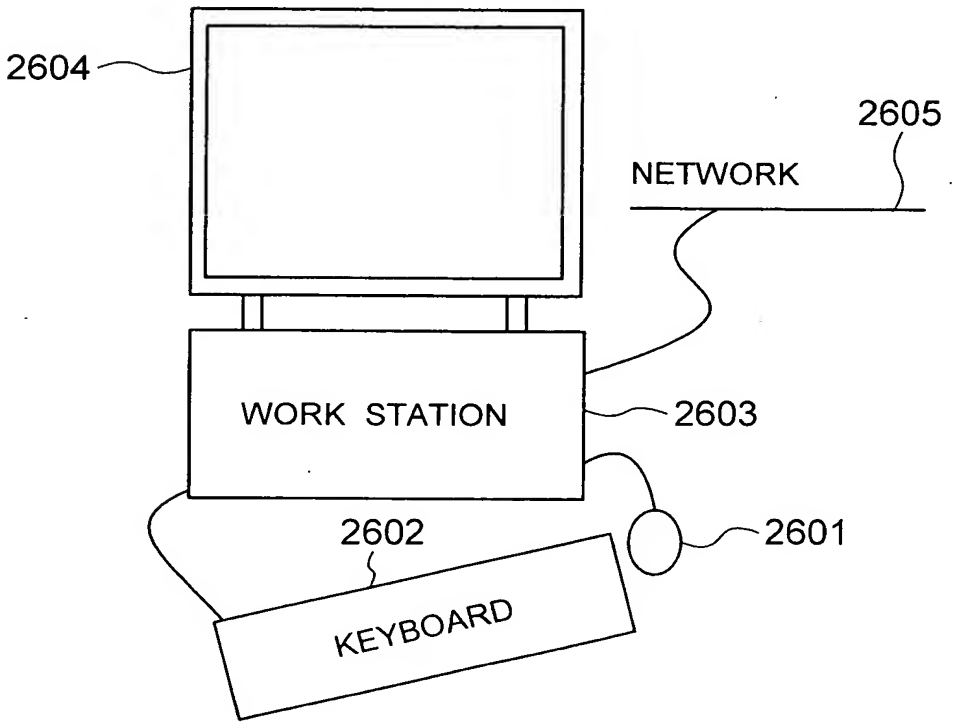
2604
2605
NETWORK
WORK STATION
2603
2602
2601
KEYBOARD

FIG. 27A

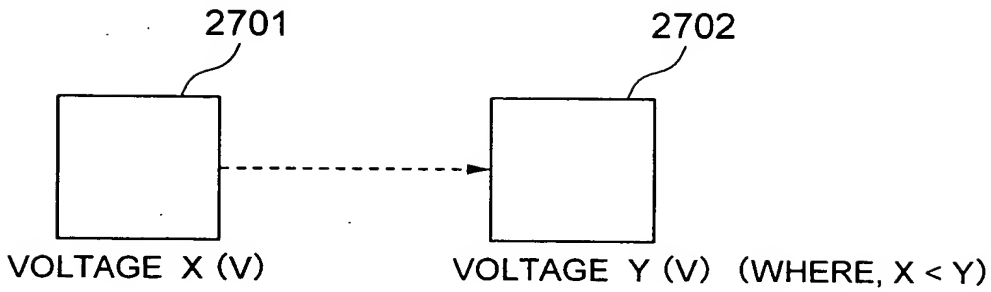

FIG. 27B

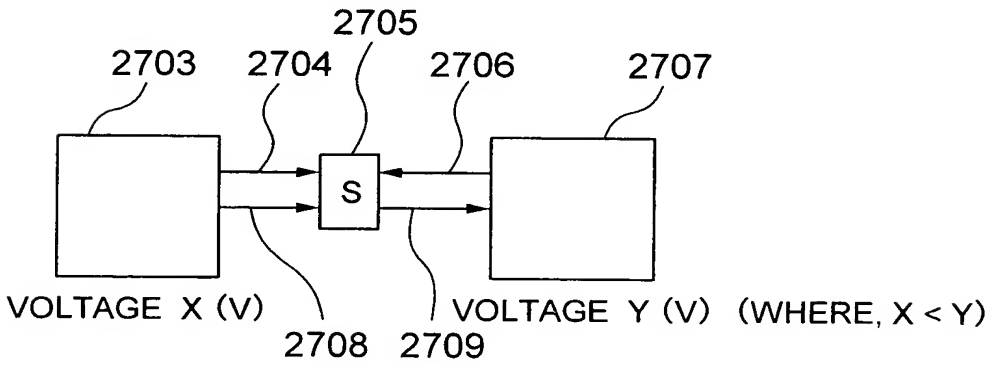

FIG. 27C